19-3279; Rev 3; 3/06

EVALUATION KIT AVAILABLE

Low-Voltage DDR Linear Regulator

General Description

The MAX1510 DDR linear regulator sources and sinks up to 3A peak (typ) using internal n-channel MOSFETs. This linear regulator delivers an accurate 0.5V to 1.5V output from a low-voltage power input (V_{IN} = 1.1V to 3.6V). The MAX1510 uses a separate 3.3V bias supply to power the control circuitry and drive the internal n-channel MOSFETs.

The MAX1510 provides current and thermal limits to prevent damage to the linear regulator. Additionally, the MAX1510 generates a power-good (PGOOD) signal to indicate that the output is in regulation. During start-up, PGOOD remains low until the output is in regulation for 2ms (typ). The internal soft-start limits the input surge current.

The MAX1510 powers the active-DDR termination bus that requires a tracking input reference. The MAX1510 can also be used in low-power chipsets and graphics processor cores that require dynamically adjustable output voltages. The MAX1510 is available in a 10-pin 3mm x 3mm thin DFN package.

Applications

Notebook/Desktop Computers

DDR Memory Termination

Active Termination Buses

Graphics Processor Core Supplies

Chipset/RAM Supplies as Low as 0.5V

Features

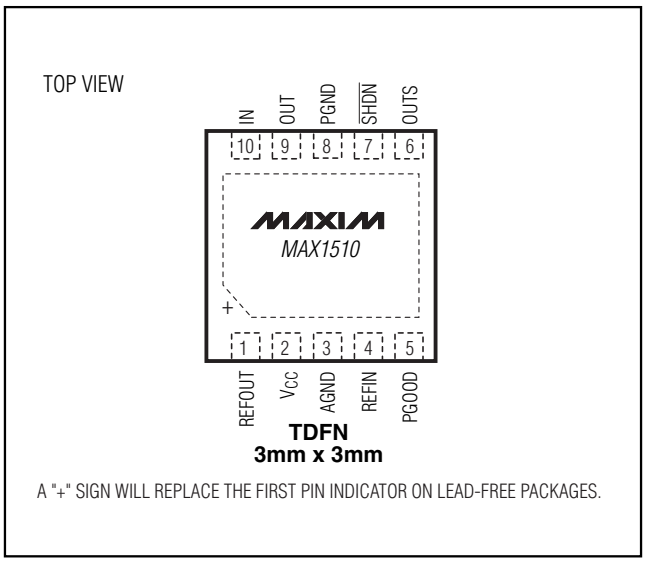
- **Internal Power MOSFETs with Current Limit (3A typ)**
- **Fast Load-Transient Response**
- **External Reference Input with Reference Output Buffer**
- **1.1V to 3.6V Power Input**
- **±15mV (max) Load-Regulation Error**
- **Thermal Fault Protection**
- **Shutdown Input**
- **Power-Good Window Comparator with 2ms (typ) Delay**
- **Small, Low-Profile 10-Pin 3mm x 3mm TDFN Package**
- **Ceramic or Polymer Output Capacitors**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK	PKG CODE
MAX1510ETB	-40°C to +85°C	10 TDFN (3mm x 3mm)	ABD	T1033-1
MAX1510ETB+	-40°C to +85°C	10 TDFN (3mm x 3mm)	ABD	T1033-1

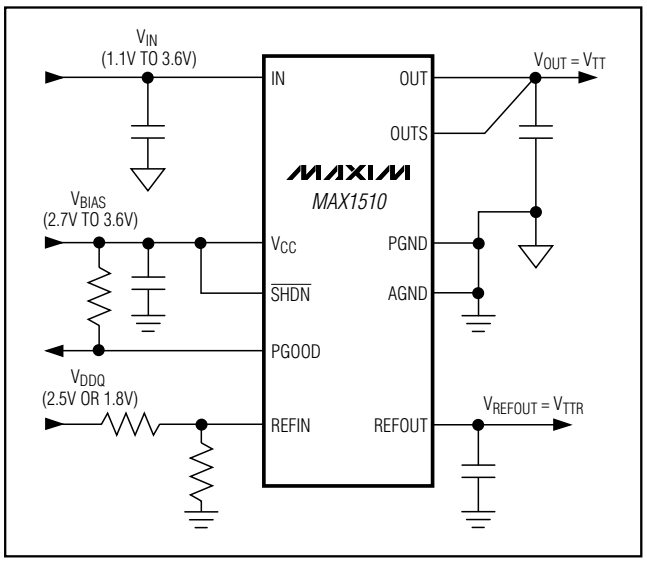
+ Denotes lead-free package.

Pin Configuration



A "+" SIGN WILL REPLACE THE FIRST PIN INDICATOR ON LEAD-FREE PACKAGES.

Typical Operating Circuit



Low-Voltage DDR Linear Regulator

ABSOLUTE MAXIMUM RATINGS

IN to PGND .....-0.3V to +4.3V
OUT to PGND .....-0.3V to (V_{IN} + 0.3V)
OUTS to AGND .....-0.3V to (V_{IN} + 0.3V)
V_{CC} to AGND .....-0.3V to +4.3V
REFIN, REFOUT, $\overline{SHDN}$, PGOOD to AGND ..-0.3V to (V_{CC} + 0.3V)
PGND to AGND .....-0.3V to +0.3V
REFOUT Short Circuit to AGND .....Continuous
OUT Continuous RMS Current: 100s .....±1.6A
1s .....±2.5A

Continuous Power Dissipation (T_A = +70°C)
10-Pin 3mm x 3mm Thin DFN
(derated 24.4mW/°C above +70°C).....1951mW
Operating Temperature Range
MAX1510ETB.....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 1.8V, V_{CC} = 3.3V, V_{REFIN} = V_{OUTS} = 1.25V, $\overline{SHDN}$ = V_{CC}, circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A= +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	Power input		1.1		3.6	V
	V_{CC}	Bias supply		2.7		3.6	
Quiescent Supply Current (V_{CC})	I_{CC}	Load = 0, V_{REFIN} > 0.45V			0.7	1.3	mA
Shutdown Supply Current (V_{CC})	$I_{CC(SHDN)}$	$\overline{SHDN}$ = GND, V_{REFIN} > 0.45V			350	600	µA
		$\overline{SHDN}$ = GND, REFIN = GND			50	100	µA
Quiescent Supply Current (V_{IN})	I_{IN}	Load = 0			0.4	10	mA
Shutdown Supply Current (V_{IN})	$I_{IN(SHDN)}$	$\overline{SHDN}$ = GND			0.1	10	µA
Feedback-Voltage Error	V_{OUTS}	REFIN to OUTS, I_{OUT} = ±200mA	T_A = 25°C	-4	0	+4	mV
			T_A = -40°C to +85°C	-6		+6	
Load-Regulation Error		-1A ≤ I_{OUT} ≤ +1A		-15		+15	mV
Line-Regulation Error		1.4V ≤ V_{IN} ≤ 3.3V, I_{OUT} = ±100mA			1		mV
OUTS Input Bias Current	I_{OUTS}			-1		+1	µA
OUTPUT							
Output Adjust Range				0.5		1.5	V
OUT On-Resistance		High-side MOSFET (source) (I_{OUT} = 0.1A)			0.16	0.25	Ω
		Low-side MOSFET (sink) (I_{OUT} = -0.1A)			0.10	0.25	
Output Current Slew Rate		C_{OUT} = 100µF, I_{OUT} = 0.1A to 2A			3		A/µs
OUT Power-Supply Rejection Ratio	PSRR	10Hz < f < 10kHz, I_{OUT} = 200mA, C_{OUT} = 100µF			80		dB
OUT to OUTS Resistance	R_{OUTS}				12		kΩ
Discharge MOSFET On-Resistance	$R_{DISCHARGE}$	$\overline{SHDN}$ = GND			8		Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 1.8V, V_{CC} = 3.3V, V_{REFIN} = V_{OUTS} = 1.25V, $\overline{SHDN}$ = V_{CC}, circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A= +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE						
REFIN Voltage Range	V_{REFIN}		0.5		1.5	V
REFIN Input Bias Current	I_{REFIN}		-1		+1	µA
REFIN Undervoltage-Lockout Voltage		Rising edge, hysteresis = 75mV		0.35	0.45	V
REFOUT Voltage	V_{REFOUT}	V_{CC} = 3.3V, I_{REFOUT} = 0	V_{REFIN} -0.01	V_{REFIN}	V_{REFIN} +0.01	V
REFOUT Load Regulation	ΔV_{REFOUT}	I_{REFOUT} = ±5mA	-20		+20	mV
FAULT DETECTION						
Thermal-Shutdown Threshold	T_{SHDN}	Rising edge, hysteresis = 15°C		+165		°C
V_{CC} Undervoltage-Lockout Threshold	V_{UVLO}	Rising edge, hysteresis = 100mV	2.45	2.55	2.65	V
IN Undervoltage-Lockout Threshold		Rising edge, hysteresis = 55mV		0.9	1.1	V
Current-Limit Threshold	I_{LIMIT}		1.8	3	4.2	A
Soft-Start Current-Limit Time	t_{SS}			200		µs
INPUTS AND OUTPUTS						
PGOOD Lower Trip Threshold		With respect to feedback threshold, hysteresis = 12mV	-200	-150	-100	mV
PGOOD Upper Trip Threshold		With respect to feedback threshold, hysteresis = 12mV	100	150	200	mV
PGOOD Propagation Delay	t_{PGOOD}	OUTS forced 25mV beyond PGOOD trip threshold	5	10	35	µs
PGOOD Startup Delay		Startup rising edge, OUTS within ±100mV of the feedback threshold	1	2	3.5	ms
PGOOD Output Low Voltage		I_{SINK} = 4mA			0.3	V
PGOOD Leakage Current	I_{PGOOD}	OUTS = REFIN (PGOOD high impedance), PGOOD = V_{CC} + 0.3V			1	µA
$\overline{SHDN}$ Logic Input Threshold		Logic high			2.0	V
		Logic low	0.8			V
$\overline{SHDN}$ Logic Input Current		$\overline{SHDN}$ = V_{CC} or GND	-1		+1	µA

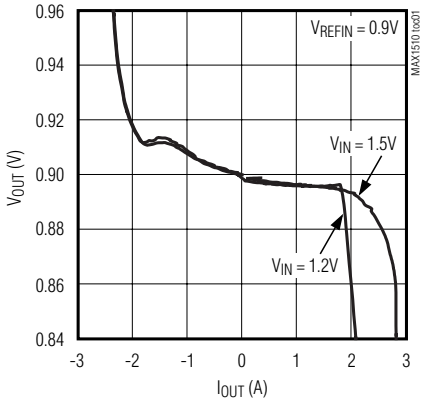
Note 1: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical-quality-control (SQC) methods.

Low-Voltage DDR Linear Regulator

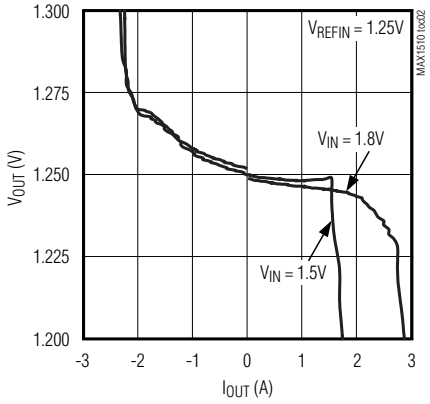
Typical Operating Characteristics

(Circuit of Figure 1. T_A = +25°C, unless otherwise noted.)

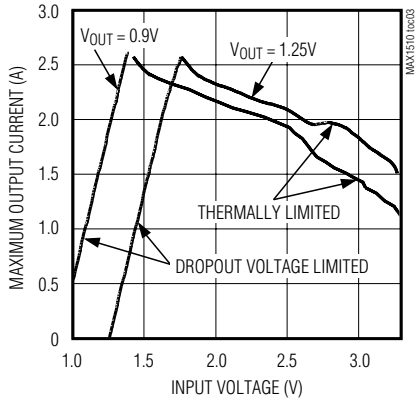
OUTPUT LOAD REGULATION



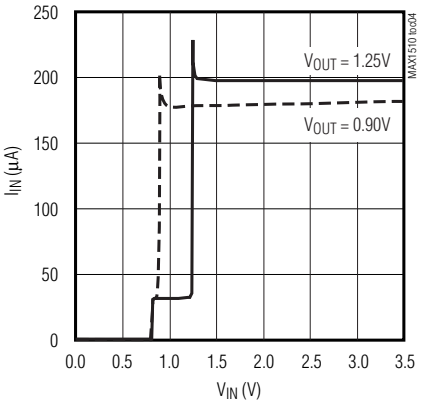
OUTPUT LOAD REGULATION



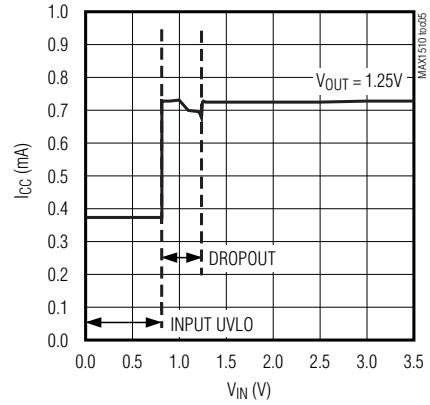
MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



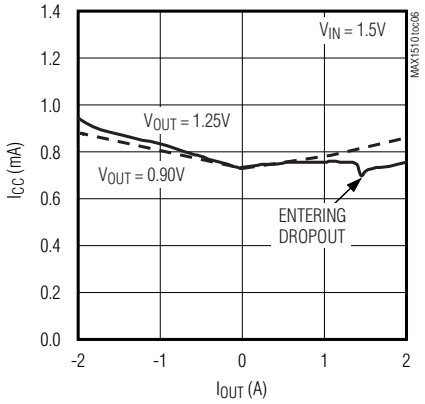
INPUT CURRENT (I_{IN}) vs. INPUT VOLTAGE (V_{IN})



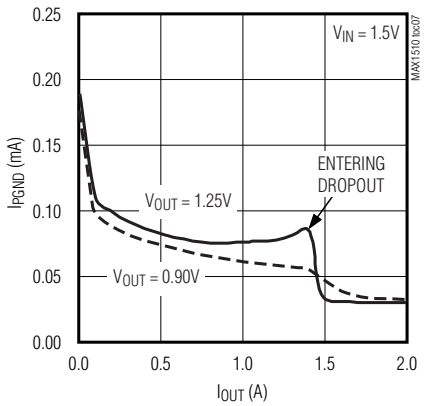
BIAS CURRENT (I_{CC}) vs. INPUT VOLTAGE (V_{IN})



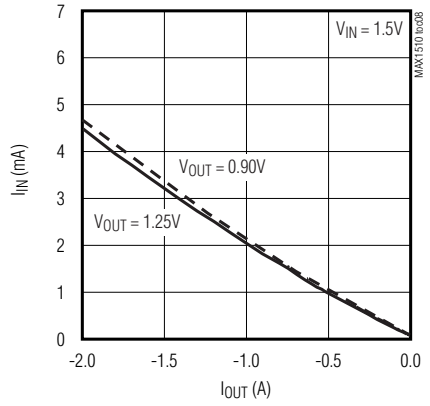
BIAS CURRENT (I_{CC}) vs. LOAD CURRENT (I_{OUT})



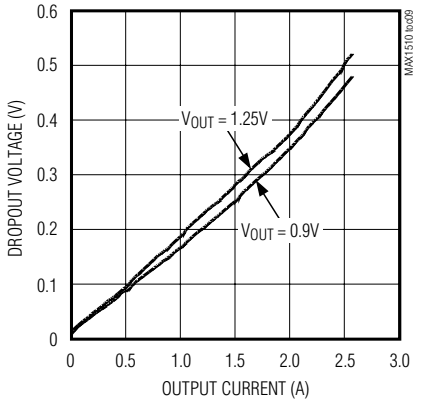
POWER GROUND CURRENT (I_{PGND}) vs. SOURCE LOAD CURRENT (I_{OUT})



INPUT CURRENT (I_{IN}) vs. SINK LOAD CURRENT (I_{OUT})



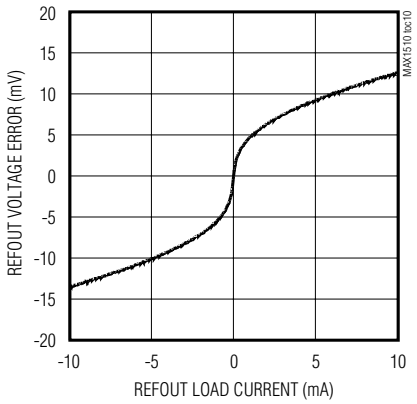
DROPOUT VOLTAGE vs. OUTPUT CURRENT



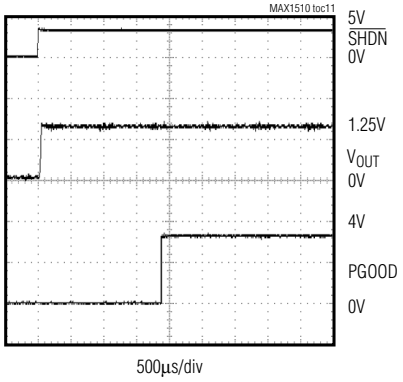
Typical Operating Characteristics (continued)

(Circuit of Figure 1. T_A = +25°C, unless otherwise noted.)

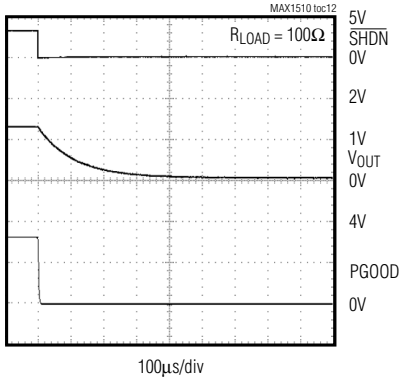
REFOUT VOLTAGE ERROR vs. REFOUT LOAD CURRENT



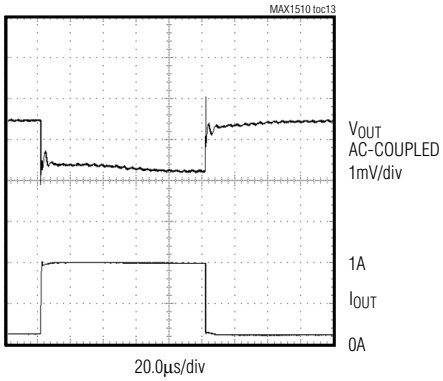
STARTUP WAVEFORM



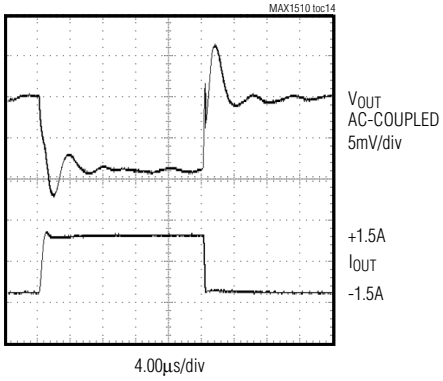
SHUTDOWN WAVEFORM



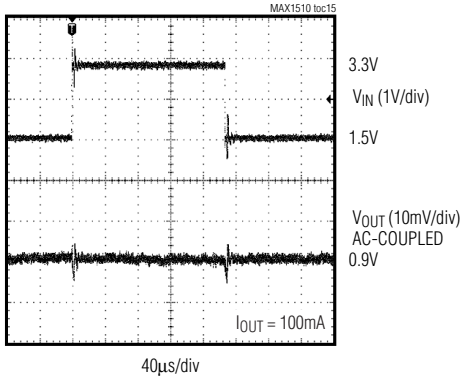
SOURCE LOAD TRANSIENT



SOURCE/SINK LOAD TRANSIENT



LINE TRANSIENT

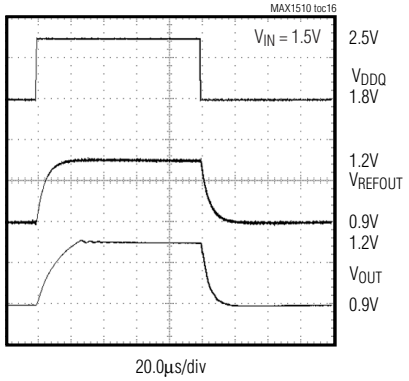


Low-Voltage DDR Linear Regulator

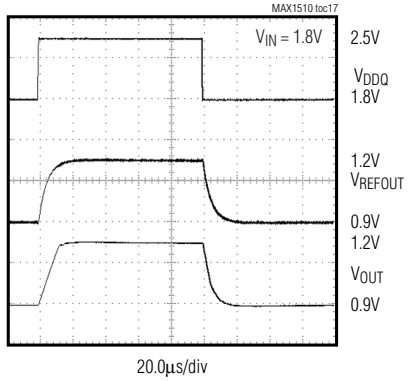
Typical Operating Characteristics (continued)

(Circuit of Figure 1. T_A = +25°C, unless otherwise noted.)

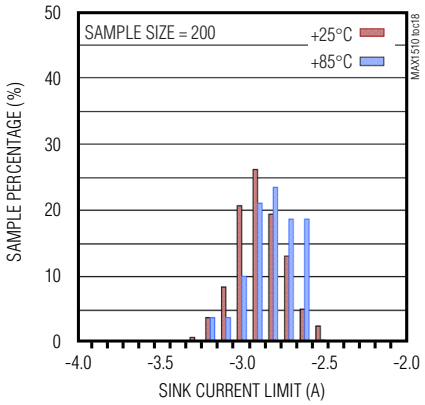
DYNAMIC OUTPUT-VOLTAGE TRANSIENT



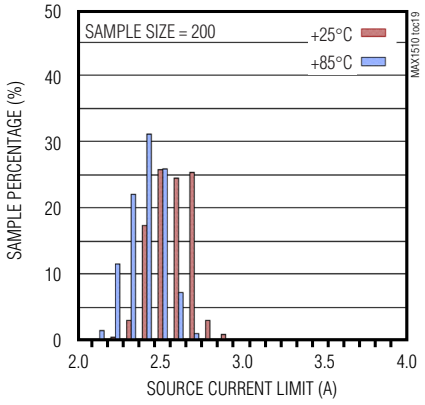
DYNAMIC OUTPUT-VOLTAGE TRANSIENT



SINK CURRENT-LIMIT DISTRIBUTION



SOURCE CURRENT-LIMIT DISTRIBUTION



Pin Description

PIN	NAME	FUNCTION
1	REFOUT	Buffered Reference Output. The output of the unity-gain reference input buffer sources and sinks over 5mA. Bypass REFOUT to AGND with a 0.33µF or greater ceramic capacitor.
2	V_{CC}	Analog Supply Input. Connect to the system supply voltage (+3.3V). Bypass V_{CC} to AGND with a 1µF or greater ceramic capacitor.
3	AGND	Analog Ground. Connect the backside pad to AGND.
4	REFIN	External Reference Input. REFIN sets the output regulation voltage ($V_{OUTS} = V_{REFIN}$).
5	PGOOD	Open-Drain Power-Good Output. PGOOD is low when the output voltage is more than 150mV (typ) above or below the regulation point, during soft-start, and when shut down. 2ms after the output reaches the regulation voltage during startup, PGOOD becomes high impedance.
6	OUTS	Output Sense Input. The OUTS regulation level is set by the voltage at REFIN. Connect OUTS to the remote DDR termination bypass capacitors. OUTS is internally connected to OUT through a 12kΩ resistor.
7	$\overline{SHDN}$	Shutdown Control Input. Connect to V_{CC} for normal operation. Connect to analog ground to shut down the linear regulator. The reference buffer remains active in shutdown.
8	PGND	Power Ground. Internally connected to the output sink MOSFET.
9	OUT	Output of the Linear Regulator
10	IN	Power Input. Internally connected to the output source MOSFET.

Detailed Description

The MAX1510 is a low-voltage, low-dropout DDR termination linear regulator with an external bias supply input and a buffered reference output (see Figures 1 and 2). V_{CC} is powered by a 2.7V to 3.6V supply that is commonly available in laptop and desktop computers. The 3.3V bias supply drives the gate of the internal pass transistor, while a lower voltage input at the drain of the transistor (IN) is regulated to provide V_{OUT}. By using separate bias and power inputs, the MAX1510 can drive an n-channel high-side MOSFET and use a lower input voltage to provide better efficiency.

The MAX1510 regulates its output voltage to the voltage at REFIN. When used in DDR applications as a termination supply, the MAX1510 delivers 1.25V or 0.9V at 3A peak (typ) from an input voltage of 1.1V to 3.6V. The MAX1510 sinks up to 3A peak (typ) as required in a termination supply. The MAX1510 provides shoot-through protection, ensuring that the source and sink MOSFETs do not conduct at the same time, yet produces a fast source-to-sink load transient.

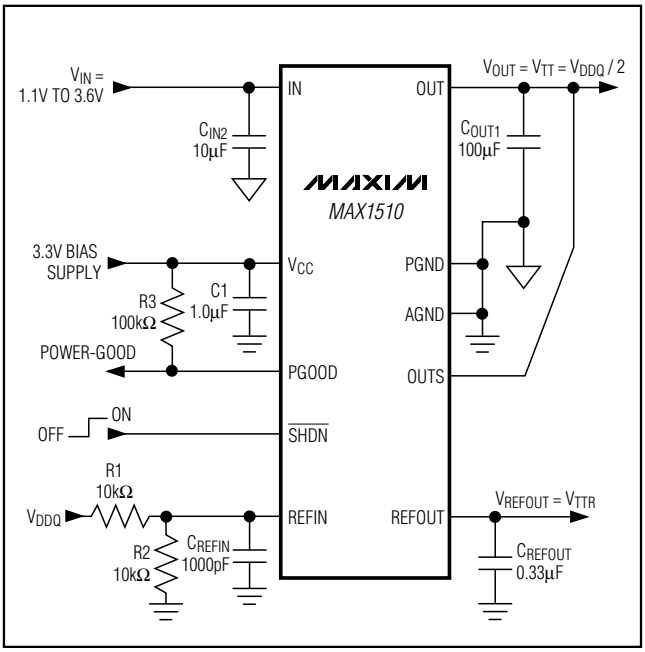


Figure 1. Standard Application Circuit

Low-Voltage DDR Linear Regulator

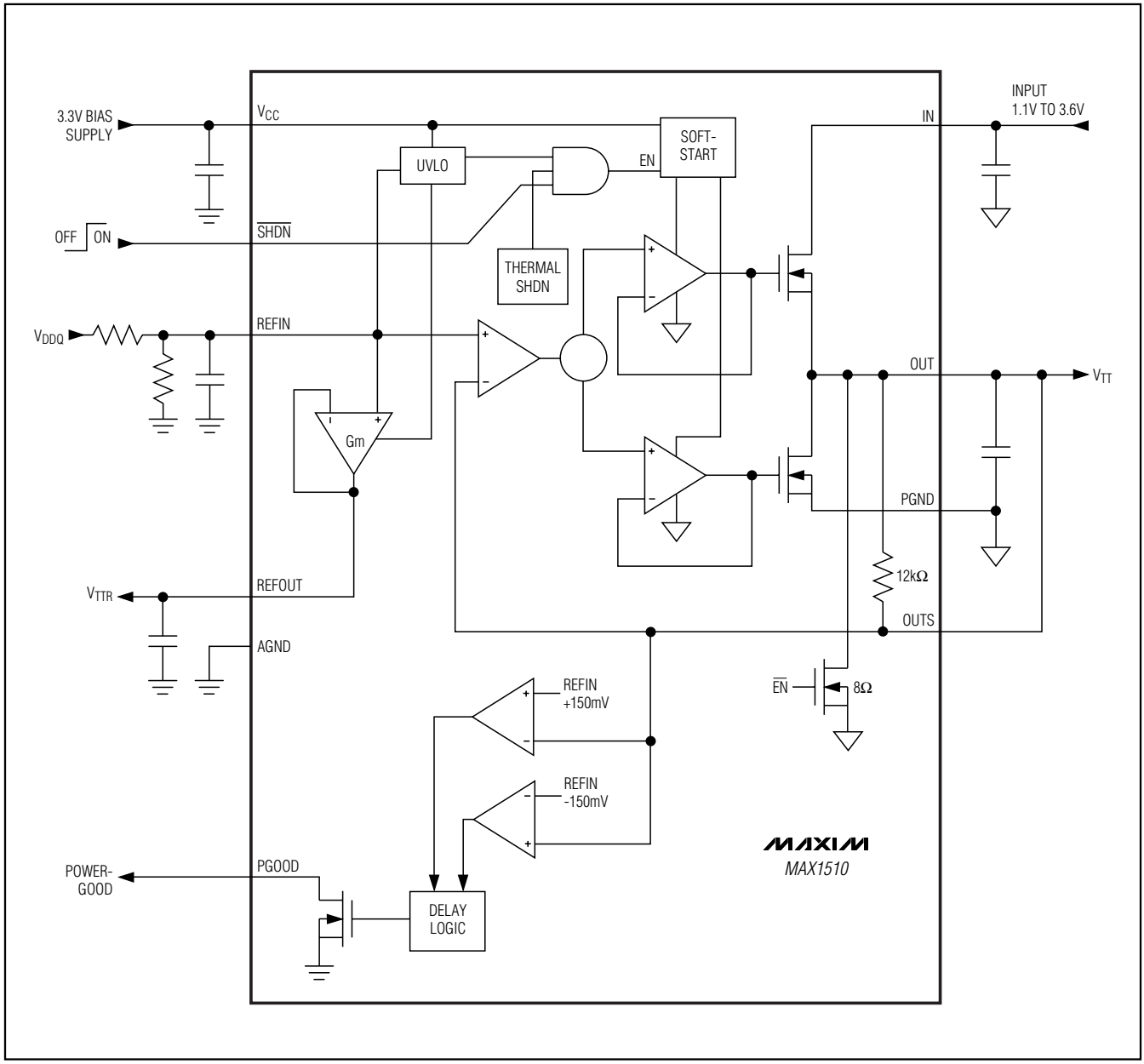


Figure 2. Functional Diagram

The MAX1510 features an open-drain PGOOD output that transitions high 2ms after the output initially reaches regulation. PGOOD goes low within 10µs of when the output goes out of regulation by ±150mV. The MAX1510 features current- and thermal-limiting circuitry to prevent damage during fault conditions.

3.3V Bias Supply (V_{CC})

The V_{CC} input powers the control circuitry and provides the gate drive to the pass transistor. This improves efficiency by allowing V_{IN} to be powered from a lower supply voltage. Power V_{CC} from a well-regulated 3.3V supply. Current drawn from the V_{CC} supply remains relatively constant with variations in V_{IN} and load current. Bypass V_{CC} with a 1µF or greater ceramic capacitor as close to the device as possible.

V_{CC} Undervoltage Lockout (UVLO)

The V_{CC} input undervoltage-lockout (UVLO) circuitry ensures that the regulator starts up with adequate voltage for the gate-drive circuitry to bias the internal pass transistor. The UVLO threshold is 2.55V (typ). V_{CC} must remain above this level for proper operation.

Power Supply Input (IN)

IN provides the source current for the linear regulator's output, OUT. IN connects to the drain of the internal n-channel power MOSFET. IN can be as low as 1.1V, minimizing power dissipation. The input UVLO prohibits operation below 0.8V (typ). Bypass IN with a 10µF or greater capacitor as close to the device as possible.

Reference Input (REFIN)

The MAX1510 regulates OUTS to the voltage set at REFIN, making the MAX1510 ideal for memory applications where the termination supply must track the supply voltage. Typically, REFIN is set by an external resistive voltage-divider connected to the memory supply (V_{DDQ}) as shown in Figure 1.

The maximum output voltage of 1.5V is limited by the gate-drive voltage of the internal n-channel power transistor.

Buffered Reference Output (REFOUT)

REFOUT is a unity-gain transconductance amplifier that generates the DDR reference supply. It sources and sinks greater than 5mA. The reference buffer is typically connected to ceramic bypass capacitors (0.33µF to 1.0µF). REFOUT is active when V_{REFIN} > 0.45V and V_{CC} is above V_{UVLO}. REFOUT is independent of $\overline{SHDN}$.

Shutdown

Drive $\overline{SHDN}$ low to disable the error amplifier, gate-drive circuitry, and pass transistor (Figure 2). In shutdown, OUT is terminated to GND with an 8Ω MOSFET. REFOUT is independent of $\overline{SHDN}$. Connect $\overline{SHDN}$ to V_{CC} for normal operation.

Current Limit

The MAX1510 features source and sink current limits to protect the internal N-channel MOSFETs. The source and sink MOSFETs have a typical 3A current limit (1.8A min). This current limit prevents damage to the internal power transistors, but the device can enter thermal shutdown if the power dissipation increases the die temperature above +165°C (see the *Thermal-Overload Protection* section).

Soft-Start Current Limit

Soft-start gradually increases the internal source current limit to reduce input surge currents at startup. Full-source current limit is available after the 200µs soft-start timer has expired. The soft-start current limit is given by:

$$I_{LIMIT(SS)} = \frac{I_{LIMIT} \times t}{t_{SS}}$$

where I_{LIMIT} and t_{SS} are from the *Electrical Characteristics.*

Thermal-Overload Protection

Thermal-overload protection prevents the linear regulator from overheating. When the junction temperature exceeds +165°C, the linear regulator and reference buffer are disabled, allowing the device to cool. Normal operation resumes once the junction temperature cools by 15°C. Continuous short-circuit conditions result in a pulsed output until the overload is removed. A continuous thermal-overload condition results in a pulsed output. For continuous operation, do not exceed the absolute maximum junction-temperature rating of +150°C.

Low-Voltage DDR Linear Regulator

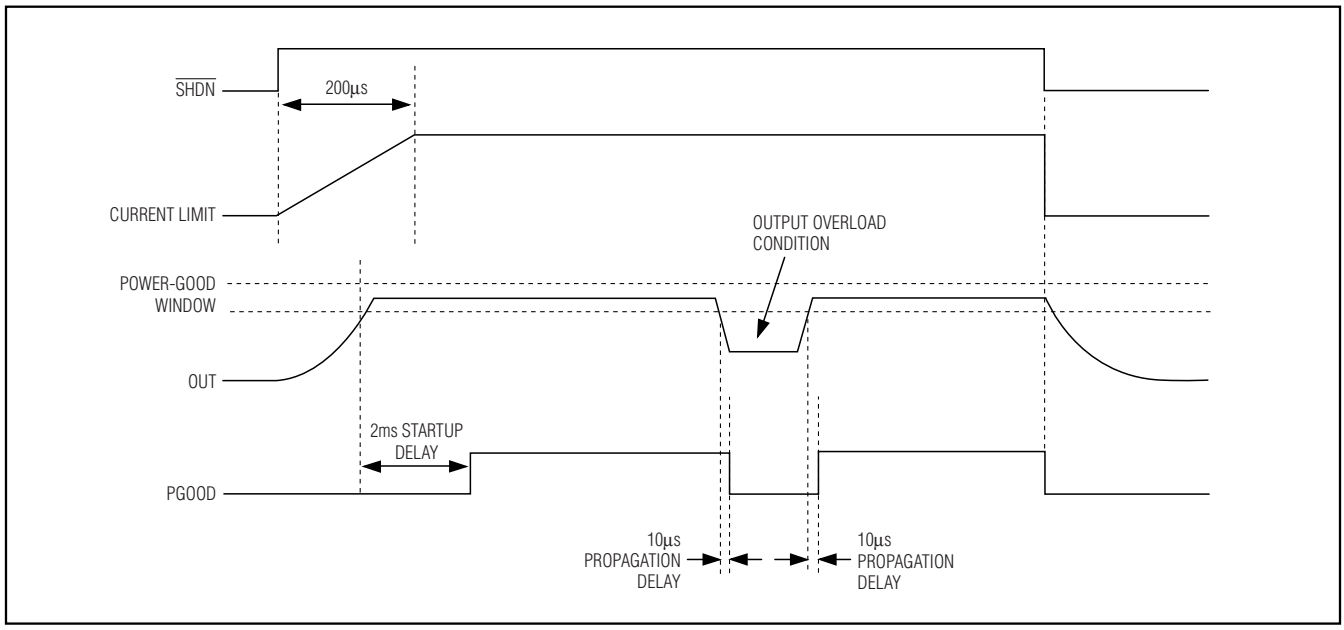


Figure 3. MAX1510 PGOOD and Soft-Start Waveforms

Power-Good (PGOOD)

The MAX1510 provides an open-drain PGOOD output that goes high 2ms (typ) after the output initially reaches regulation during startup. PGOOD transitions low 10µs after the output goes out of regulation by ±150mV, or when the device enters shutdown. Connect a pullup resistor from PGOOD to V_{CC} for a logic-level output. Use a 100kΩ resistor to minimize current consumption.

Applications Information

Dynamic Output-Voltage Transitions

By changing the voltage at REFIN, the MAX1510 can be used in applications that require dynamic output-voltage changes between two set points (graphics processors). Figure 4 shows a dynamically adjustable resistive voltage-divider network at REFIN. Using an external signal MOSFET, a resistor can be switched in and out of the REFIN resistor-divider, changing the voltage at REFIN. The two output voltages are determined by the following equations:

$$V_{OUT(LOW)} = V_{REF}\left(\frac{R2}{R1 + R2}\right)$$

$$V_{OUT(HIGH)} = V_{REF}\left[\frac{(R2 + R3)}{R1 + (R2 + R3)}\right]$$

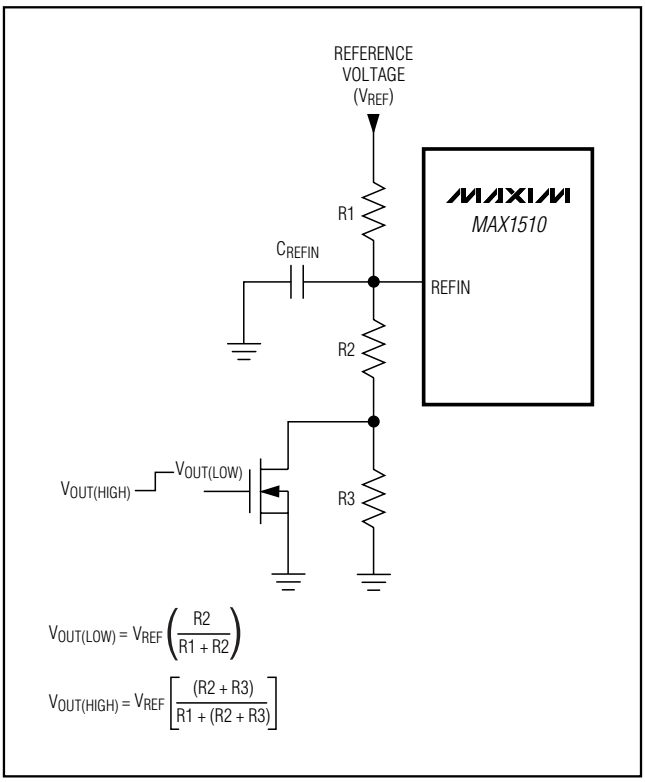


Figure 4. Dynamic Output-Voltage Change

For a step voltage change at REFIN, the rate of change of the output voltage is limited by the total output capacitance, the current limit, and the load during the transition. Adding a capacitor across REFIN and AGND filters noise and controls the rate of change of the REFIN voltage during dynamic transitions. With the additional capacitance, the REFIN voltage slews between the two set points with a time constant given by $R_{EQ} \times C_{REFIN}$, where R_{EQ} is the equivalent parallel resistance seen by the slew capacitor.

Operating Region and Power Dissipation

The maximum power dissipation of the MAX1510 depends on the thermal resistance of the 10-pin TDFN package and the circuit board, the temperature difference between the die and ambient air, and the rate of airflow. The power dissipated in the device is:

$$P_{SRC} = I_{SRC} \times (V_{IN} - V_{OUT})$$
$$P_{SINK} = I_{SINK} \times V_{OUT}$$

The resulting maximum power dissipation is:

$$P_{DIS(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JC} + \theta_{CA}}$$

where $T_{J(MAX)}$ is the maximum junction temperature (+150°C), T_A is the ambient temperature, θ_{JC} is the thermal resistance from the die junction to the package case, and θ_{CA} is the thermal resistance from the case through the PC board, copper traces, and other materials to the surrounding air. For optimum power dissipation, use a large ground plane with good thermal contact to the backside pad, and use wide input and output traces.

When 1 square inch of copper is connected to the device, the maximum allowable power dissipation of a 10-pin DFN package is 1951mW. The maximum power dissipation is derated by 24.4mW/°C above T_A = +70°C. Extra copper on the PC board increases thermal mass and reduces thermal resistance of the board. Refer to the MAX1510 evaluation kit for a layout example.

The MAX1510 delivers up to 3A and operates with input voltages up to 3.6V, but not simultaneously. High output currents can only be achieved when the input-output differential voltages are low (Figure 5).

Dropout Operation

A regulator's minimum input-to-output voltage differential (dropout voltage) determines the lowest usable supply voltage. Because the MAX1510 uses an n-channel pass transistor, the dropout voltage is a function of the drain-to-source on-resistance ($R_{DS(ON)}$ = 0.25Ω max) multiplied by the load current (see the *Typical Operating Characteristics*):

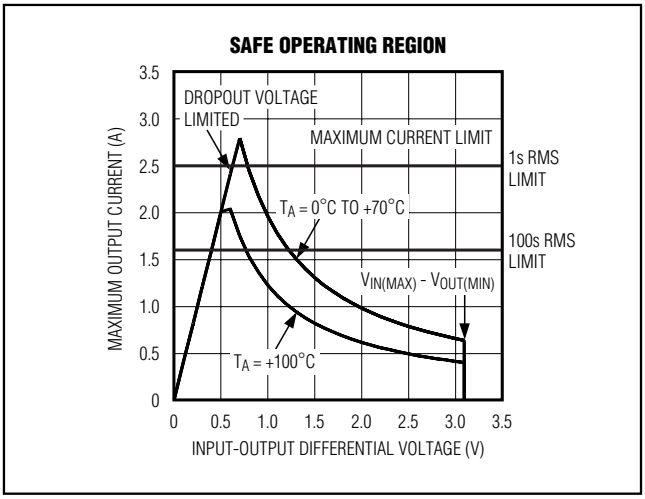


Figure 5. Power Operating Region—Maximum Output Current vs. Input-Output Differential Voltage

$$V_{DROPOUT} = R_{DS(ON)} \times I_{OUT}$$

For low output-voltage applications the sink current is limited by the output voltage and the $R_{DS(ON)}$ of the MOSFET.

Input Capacitor Selection

Bypass IN to PGND with a 10µF or greater ceramic capacitor. Bypass V_{CC} to AGND with a 1µF ceramic capacitor for normal operation in most applications. Typically, the LDO is powered from the output of a step-down controller (memory supply) that has additional bulk capacitance (polymer or tantalum) and distributed ceramic capacitors.

Output Capacitor Selection

The MAX1510 output stability is independent of the output capacitance for C_{OUT} from 10µF to 220µF. Capacitor ESR between 2mΩ and 50mΩ is needed to maintain stability. Within the recommended capacitance and ESR limits, the output capacitor should be chosen to provide good transient response.

$$\Delta I_{OUT(P-P)} \times ESR = \Delta V_{OUT(P-P)}$$

where $\Delta I_{OUT(P-P)}$ is the maximum peak-to-peak load-current step (typically equal to the maximum source load plus the maximum sink load), and $\Delta V_{OUT(P-P)}$ is the allowable peak-to-peak voltage tolerance.

Using larger output capacitance can improve efficiency in applications where the source and sink currents change rapidly. The capacitor acts as a reservoir for the rapid source and sink currents, so no extra current is supplied by the MAX1510 or discharged to ground, improving efficiency.

Low-Voltage DDR Linear Regulator

Noise, PSRR, and Transient Response

The MAX1510 operates with low-dropout voltage and low quiescent current in notebook computers while maintaining good noise, transient response, and AC rejection specifications. Improved supply-noise rejection and transient response can be achieved by increasing the values of the input and output capacitors. Use passive filtering techniques when operating from noisy sources.

The MAX1510 load-transient response graphs (see the *Typical Operating Characteristics*) show two components of the output response: a DC shift from the output impedance due to the load-current change and the transient response. A typical transient response for a step change in the load current from -1.5A to +1.5A is 10mV. Increasing the output capacitor's value and decreasing the ESR attenuate the overshoot.

PC Board Layout Guidelines

The MAX1510 requires proper layout to achieve the intended output power level and low noise. Proper layout involves the use of a ground plane, appropriate component placement, and correct routing of traces using appropriate trace widths. Refer to the MAX1510 evaluation kit for a layout example.

1) Minimize high-current ground loops. Connect the ground of the device, the input capacitor, and the output capacitor together at one point.
2) To optimize performance, a ground plane is essential. Use all available copper layers in applications where the device is located on a multilayer board.
3) Connect the input filter capacitor less than 10mm from IN. The connecting copper trace carries large currents and must be at least 2mm wide, preferably 5mm wide.
4) Connect the backside pad to a large ground plane. Use as much copper as necessary to decrease the thermal resistance of the device. In general, more copper provides better heatsinking capabilities.

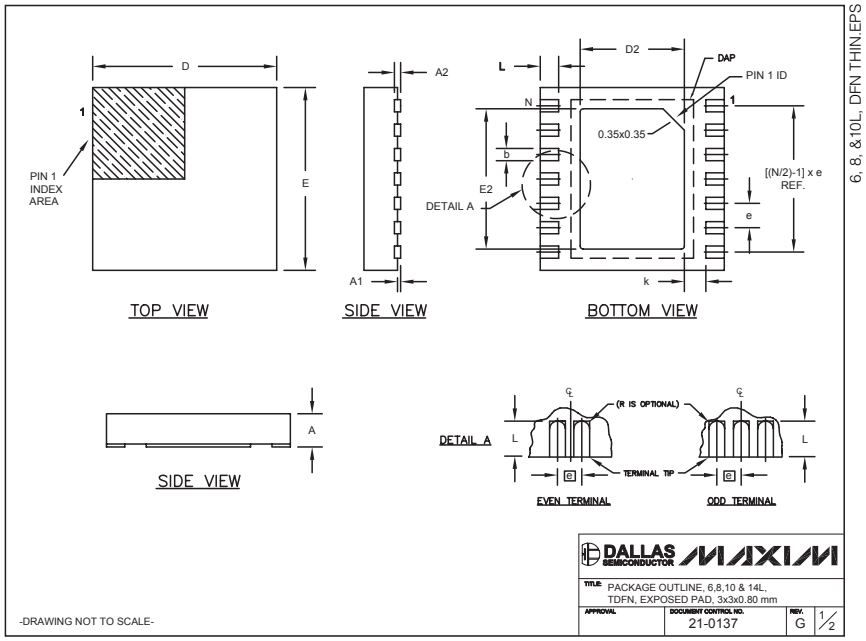
Chip Information

TRANSISTOR COUNT: 3496

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS

PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e	DOWNBONDS ALLOWED
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF	NO
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	NO
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF	YES
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF	NO
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF	YES
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF	NO

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM
TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm
APPROVAL
DOCUMENT CONTROL NO. 21-0137
REV. G
2/2